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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for nonprovisional applications under 37 CFR § 1.53(b))

Attorney Docket No.	108298531US
First Inventor or Application Identifier	David J. Corisis et al.
Title	METHOD AND APPARATUS FOR DECOUPLING CONDUCTIVE PORTIONS OF A MICROELECTRONIC DEVICE PACKAGE
Express Mail Label No.	EL404935146US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Box Patent Application, Assistant Commissioner for Patents, Washington, D.C. 20231

1. [X] Authorization for Extensions & Fee Transmittal *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [Total Pages] 21 *(preferred arrangement set forth below)*
   - Descriptive Title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [Total Sheets] 4
4. Oath or Declaration [Total Pages] 2
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)

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5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer-Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

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ACCOMPANYING APPLICATION PARTS

7. [X] Assignment Papers (cover sheet & document(s))
8. [X] 37 CFR 3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard
12. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
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16. **If a CONTINUING APPLICATION,** *check appropriate box and supply the requisite information below and in a preliminary amendment*

[ ] Continuation [ ] Divisional [ ] Continuation-In-Part (CIP) of prior Application No.: _____

Prior application information: Examiner _____ *Group / Art Unit* _____

For CONTINUATION or DIVISIONAL apps only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

[ ] Claims the benefit of Provisional Application No. _____

17. CORRESPONDENCE ADDRESS

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25096

PATENT TRADEMARK OFFICE

Respectfully submitted,

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SIGNATURE _____ Date August 23, 2000

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METHOD AND APPARATUS FOR DECOUPLING CONDUCTIVE PORTIONS OF A MICROELECTRONIC DEVICE PACKAGE

TECHNICAL FIELD

This invention relates to methods and apparatuses for decoupling conductive portions of a microelectronic device package.

BACKGROUND OF THE INVENTION

Packaged microelectronic assemblies, such as memory chips and microprocessor chips, typically include a microelectronic device mounted to a substrate and encased in a plastic protective covering. The device includes functional features, such as memory cells, processor circuits, and interconnecting circuitry. The device also typically includes bond pads electrically coupled to the functional features. The bond pads are coupled to pins or other types of terminals that extend outside the protective covering for connecting the microelectronic device to buses, circuits and/or other microelectronic assemblies.

In one conventional arrangement shown in Figure 1, a device package 20 includes a microelectronic die 50 having bond pads 51 positioned along two central axes. A conductive leadframe 30 having conductive leadfingers 31 connected by an outer rim 38 is positioned over the die 50. The leadfingers 31 are separated from the top surface of the die 20 by an insulating layer 60 on the bottom of the leadframe 30. The leadfingers 31 are electrically coupled to the corresponding bond pads 51 with wire bonds 40, and the die 50 and the leadframe 30 are encapsulated with an encapsulating material 21 (the outer periphery of the encapsulating material 21 is shown in phantom lines in Figure 1). The leadframe 30 is then trimmed along cut lines 33 and the portions of the leadfingers 31 projecting outwardly from the encapsulating material 21 are bent to form pins or other electrically conductive connectors configured to couple the package 20 to other devices or circuit elements.

Devices such as the package 20 described above with reference to Figure 1 are typically used in compact electronic products, such as laptop computers and mobile telephones. As these electronic products are made more compact, the dies 50 and the

packages 20 are also made more compact. One result of this trend is that the spacing between adjacent leadfingers 31 decreases. One problem with this result is that the signals transmitted along adjacent leadfingers 31 can become capacitively coupled . The capacitive coupling can cause signal errors in one or both of the adjacent leadfingers 31, which can adversely affect the performance and reliability of the electronic products into which the packages 20 are incorporated.

SUMMARY

The present invention is directed toward methods and apparatuses for decoupling conductive portions of a microelectronic device package. A method in accordance with one aspect of the invention includes positioning a conductive member at least proximate to a microelectronic substrate. The conductive member can include a leadframe or traces of a printed circuit board and can have first and second neighboring conductive portions with at least part of the first conductive portion separated from the neighboring second conductive portion to define an intermediate region between the two portions. The method can further include electrically coupling the first conductive portion to a first coupling site of the microelectronic substrate and electrically coupling the second conductive portion to a second coupling site of the microelectronic substrate. The method can still further include providing a dielectric material in the intermediate region between the conductive portions with the dielectric material having a dielectric constant of less than about 3.5.

The invention is also directed toward a conductive structure for coupling to a microelectronic substrate. The structure can include a conductive member having first and second conductive portions with at least a part of the first conductive portion being spaced apart from a neighboring part of the second conductive portion to define an intermediate region between the first and second conductive portions. Each conductive portion has a bond region positioned to electrically couple to a microelectronic substrate when the conductive member is positioned at least approximate to the microelectronic substrate. The structure can further include a dielectric material adjacent to the first and second conductive portions and having a dielectric constant of less than about 3.5. The dielectric material can include a pliable material positioned adjacent to opposite surfaces of the conductive portions and can

be squeezed into the intermediate region between the conductive portions where the dielectric material can fill all or part of the intermediate region.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a partially schematic, top view of a microelectronic device package in accordance with the prior art.

Figure 2 is a top isometric view of a conductive member and a dielectric material configured in accordance with an embodiment of the invention.

Figure 3 is a cross-sectional side view of an embodiment of the conductive member shown in Figure 2 taken substantially along line 3-3.

Figure 4 is a cross-sectional end view of an embodiment of the conductive member shown in Figure 2 taken substantially along line 4-4, with the conductive member mounted to a microelectronic substrate in accordance with an embodiment of the invention.

Figures 5A-5D illustrate methods for forming conductive members with dielectric materials in accordance with several embodiments of the invention.

Figure 6 is a cross-sectional end view of a microelectronic substrate coupled to a conductive assembly to form a device package in accordance with another embodiment of the invention.

Figure 7 is a cross-sectional side view of an embodiment of the package shown in Figure 6 taken substantially along line 7-7.

DETAILED DESCRIPTION

The present disclosure describes packaged microelectronic devices and methods for packaging such devices. Many specific details of certain embodiments of the invention are set forth in the following description and in Figures 2-7 to provide a thorough understanding of these embodiments. One skilled in the art, however, will understand that the present invention may have additional embodiments, or that the invention may be practiced without several of the details described below.

Figure 2 is a top isometric view of a conductive member 130 (such as a leadframe) having conductive portions 131 (such as leadfingers) and a dielectric material 160 for controlling capacitive coupling between the conductive portions 131. In one aspect of

this embodiment, each conductive portion 131 is initially supported in a fixed position relative to its neighbors by a connection portion 138 that forms a frame around the conductive portions 131. Accordingly, neighboring conductive portions 131 are separated from each other by an intermediate region 137. Each conductive portion 131 has an upper surface 134, a lower surface 135 opposite the upper surface 134, and a side surface 136 between the upper surface 134 and the lower surface 135. Each conductive portion 131 also has a bond region 132 spaced apart from the connecting portion 138 for coupling to a microelectronic substrate, as will be described in greater detail below with reference to Figure 4.

In one aspect of an embodiment shown in Figure 2, the dielectric material 160 can include an upper portion 161 adjacent to the upper surfaces 134 of the conductive portions 131, a lower portion 162 adjacent to the lower surfaces 135 of the conductive portions 131, and an intermediate portion 163 adjacent to the side surfaces 136 of the conductive portions 131 in the intermediate regions 137 between neighboring conductive portions 131. In an further aspect of this embodiment, the upper portions 161 of the dielectric material 160 do not cover the bond regions 132 of the conductive portions 131, so that electrical connections can be easily made with the bond regions 132. Alternatively, the dielectric material 160 can be initially disposed on the bond regions 132 and then removed, for example by etching, laser ablation, or other processes, before coupling the conductive member 130 to a microelectronic substrate. In still a further aspect of this embodiment, the dielectric material 160 can have an aperture 164 that extends entirely through the dielectric material 160 near the bond regions 132. Accordingly, the aperture 164 can accommodate wire bonds or other connecting structures attached to the bond regions 132, as will be described in greater detail below with reference to Figure 4.

Figure 3 is a cross-sectional, side view of an embodiment of the conductive member 130 taken substantially along line 3-3 of Figure 2. In one aspect of this embodiment, the intermediate portions 163 of the dielectric material 160 completely fill the intermediate regions 137 between neighboring conductive portions 131. In an alternate embodiment, the dielectric material 160 in the intermediate regions 137 can have gaps or voids, as will be described in greater detail below with reference to Figure 5B.

Figure 4 is a cross-sectional end view of an embodiment of the conductive member 130 taken substantially along line 4-4 of Figure 2. The conductive member 130 is

mounted to a microelectronic substrate 150 in accordance with an embodiment of the invention. In one aspect of this embodiment, the microelectronic substrate 150 has a first surface 153, a second surface 152 facing opposite the first surface 153, and a plurality of bond pads 151 or other bond sites on the second surface 152. The bond pads 151 are connected to integrated circuitry in the microelectronic substrate 150.

In one aspect of the embodiment shown in Figure 4, the conductive member 130 is positioned adjacent to the second surface 152 of the microelectronic substrate 150, with the aperture 164 aligned with the bond pads 151. Accordingly, the lower portion 162 of the dielectric material 160 is positioned adjacent to the second surface 152 of the microelectronic substrate 150. A wire bond 140 or other connective element extends between selected bond pads 151 and corresponding bond regions 132 of the conductive portions 131 to provide conductive links between the microelectronic substrate 150 and the conductive member 130. The microelectronic substrate 150, the wire bonds 140, and the conductive portions 131 are then encapsulated with an encapsulating material 121 to form a device package 120. The connecting portion 138 (Figure 2) of the conductive member 130 can then be trimmed, and external sections 139 of the conductive portions 131 outside the encapsulating material 121 can be shaped into connecting pins or other connecting structures.

One feature of an embodiment of the device package 120 and the conductive member 130 described above with reference to Figures 2-4 is that the dielectric material 160 adjacent to the conductive portions 131 can be selected to control capacitive coupling between neighboring conductive portions 131. For example, in one embodiment, the dielectric material 160 can include Teflon™ and can have a dielectric constant of from approximately 1.0 to approximately 2.0. Accordingly, the likelihood for capacitive coupling between neighboring conductive portions 131 can be reduced when compared to conventional arrangements (such as the arrangement described above with reference to Figure 1) that have relatively high dielectric encapsulating materials positioned between adjacent leadfingers. In other embodiments, the dielectric material 160 can have a dielectric constant higher than 2.0, but less than the dielectric constant of conventional encapsulating materials, which is approximately 3.5 and above.

An advantage of the relatively low dielectric constant of the dielectric material 160 is that signals transmitted along one conductive portion 131 will be less likely to affect signals transmitted along an adjacent conductive portion 131. Another advantage of this

feature is that the conductive portions 131 can be positioned more closely together than in some conventional arrangements without capacitively coupling adjacent conductive portions 131. Accordingly, the conductive member 130 can be smaller than conventional leadframes and can be suitable for use with reduced-size microelectronic substrates 150.

Figures 5A-5D schematically illustrate processes for disposing dielectric materials on conductive members in accordance with several embodiments of the invention. Referring first to Figure 5A, the dielectric material 160 can include a pliable upper layer 261 disposed adjacent to the upper surface 134 of the conductive member 130, and a pliable lower layer 262 disposed adjacent to the lower surface 135 of the conductive member 130. In a further aspect of this embodiment, each layer 261, 262 can include a low dielectric adhesive 265 that adheres the layer to the conductive member 130. Alternatively, the dielectric material 160 forming the layers 261, 262 can self-adhere to the conductive member 130. In either embodiment, the dielectric constant of the upper layer 261 can be the same as or different than the dielectric constant of the lower layer 262. In one embodiment, the dielectric material 160 can be a thermoset material that is cured after attaching it to the conductive member 130. In other embodiments, the dielectric material 160 can have other thermal characteristics.

In one aspect of an embodiment of the process shown in Figure 5A, the layers 261, 262 do not initially extend into the intermediate regions 137 between neighboring conductive portions 131. Accordingly, in a further aspect of this embodiment (shown in Figure 5B), pressure can be applied to the upper layer 261 and/or the lower layer 262 (as indicated by arrows P) to force at least a portion of the dielectric material 160 that forms the layers 261, 262 into the intermediate regions 137 between neighboring conductive portions 131. In one aspect of this embodiment, the dielectric material 160 can also be heated to encourage the movement of the dielectric material 160 into the intermediate regions 137, and/or to cure the dielectric material 160, for example, when the dielectric material 160 includes a thermoset material. Alternatively, the pressure can be applied to the dielectric material 160 at room temperature. In either embodiment, the pressure can be applied to the dielectric material 160 either before or after the conductive member 130 is positioned adjacent to the microelectronic substrate 150 (Figure 4).

In one embodiment, the dielectric material 160 can fill only a portion of the intermediate regions 137. For example, as shown in Figure 5B, voids 166 can remain in the

intermediate regions 137 after pressure has been applied to the dielectric material 160. In a further aspect of this embodiment, the process described above with reference to Figure 5B can be conducted in a controlled gas environment to control the nature of the gas residing in the voids 166. Accordingly, the gas can include air, helium, argon or other gases having a generally low dielectric constant. Alternatively, the dielectric material 160 can fill the intermediate regions 137 in their entirety (as shown in Figures 2 and 3). Accordingly, the thickness of the layers 261, 262 and the processing parameters described above can be selected to eliminate the voids 166.

An advantage of a process for forming the conductive member 130 described above with reference to Figures 5A-5B is that the layers 261, 262 of the conductive material 160 can be easily applied to the conductive member 130. For example, the layers 261, 262 can be formed into adhesive strips or pads separately from forming the conductive members 130, and can be applied to the conductive members 130 as needed. Alternatively, the layers 261, 262 can be applied to the conductive members 130 as part of the process for forming the conductive members 130, for example, by unrolling continuous strips of dielectric materials adjacent to opposite surfaces of a continuous strip of conductive members 130.

In an alternate embodiment shown schematically in Figure 5C, the dielectric material 160 is disposed on the conductive member 130 in the form of a liquid or vapor using a deposition or spray process. Accordingly, the dielectric material 160 can conform to the features of the conductive member 130 and can entirely fill the intermediate regions 137 between neighboring conductive portions 131. In one aspect of this embodiment, the dielectric material 160 can be initially deposited adjacent to the upper surface 134 of the conductive member 130 and then deposited adjacent to the lower surface 135. Alternatively, both deposition processes can take place simultaneously.

In another aspect of an embodiment of the process described above with reference to Figure 5C, at least a portion of the dielectric material 160 can be deposited on the conductive member 130 after the conductive member 130 has been mounted to the microelectronic substrate 150 (Figure 4). For example, the dielectric material 160 can be deposited adjacent to the lower surface 135 of the conductive member 130, but not the upper surface 134. The conductive member 130, with the lower surface 135 covered with the dielectric material 160, can be positioned adjacent to the microelectronic substrate 150 and wire bonded to the microelectronic substrate 150, as described above with reference to

Figure 4. An additional amount of dielectric material 160 can then be deposited on the microelectronic substrate 150, the wire bond 140 and the upper surface 134 of the conductive member 130 to fill in the intermediate regions 137 between the neighboring conductive portions 131 and encapsulate the wire bonds 140. In a further aspect of this embodiment, the encapsulating material 121 described above with reference to Figure 4 can be eliminated and the functions provided by the encapsulating material 121 (for example, protecting the microelectronic substrate 150 and the wire bonds 140 from contaminants) can be provided by the dielectric material 160 alone. An advantage of this arrangement is that the dielectric material 160 can prevent or control capacitive coupling between adjacent conductive portions 131 of the conductive member 130 and can protect and encapsulate the microelectronic substrate 150.

Figure 5D schematically illustrates a process in accordance with yet another embodiment of the invention in which the conductive member 130 is dipped into a reservoir 180 containing the dielectric material 160. In one aspect of this embodiment, the entire conductive member 130 can be dipped into the dielectric material 160 to dispose the dielectric material in the intermediate regions 137 and adjacent to the upper surface 134 and the lower surface 135 of the conductive member 130. Alternatively, the conductive member 130 can be initially dipped into the reservoir 180 with the lower surface 135 facing the dielectric material 160, and subsequently inverted and re-dipped into the reservoir 180 with the upper surface 134 facing the dielectric material 160. In either embodiment, the dielectric material can be removed from the bond region 132 (Figure 2) by etching or other processes. Alternatively, the bond regions 132 can be protected with a removable covering prior to dipping the conductive member 130 in the dielectric material 160.

Figure 6 is a cross-sectional end view of a microelectronic substrate 350 coupled to a conductive assembly 330 to form a packaged device 320 in accordance with another embodiment of the invention. Figure 7 is a cross-sectional side view of the package 320 taken substantially along line 7-7 of Figure 6. Referring now to Figures 6 and 7, the microelectronic substrate 350 includes substrate bond pads 351 coupled to internal features (not shown). The microelectronic substrate 350 is supported by a package support member 370a, such as a printed circuit board (PCB) that includes an aperture 383 aligned with the substrate bond pads 351. The package support member 370a also includes a conductive

assembly 330 facing away from the microelectronic substrate 350 and configured to be coupled to the substrate bond pads 351.

In one aspect of an embodiment shown in Figures 6 and 7, the conductive assembly 330 includes a network or array of conductive traces 331. The conductive traces 331 are connected between inner bond pads 353a adjacent to the aperture 383 and outer bond pads 353b. Wire bonds 340 are connected between the inner bond pads 353a and the substrate bond pads 351 to link the internal features of the microelectronic substrate 350 to the conductive assembly 330. The microelectronic substrate 350, the package support member 370a and the wire bonds 340 are at least partially encased in an encapsulating material 321 to form the packaged device 320. The packaged device 320 can be connected to another, larger support member 370b by coupling solder balls 371 between the outer bond pads 353b of the package support member 370a and corresponding bond pads 353c of the other support member 370b.

In one aspect of an embodiment shown in Figures 6 and 7, each trace 331 has an upper surface 334, a lower surface 335 opposite the upper surface 334, and a side surface 336 between the upper surface 334 and the lower surface 335. The side surfaces 336 of neighboring traces 331 are spaced apart to define intermediate regions 337. A dielectric material 360 can be positioned adjacent to the traces 331 to cover one or more of the surfaces of the traces 331. For example, in one embodiment, the dielectric material 360 can include a lower portion 362 adjacent to the lower surface 335 of the conductive traces 331, and an intermediate portion 363 in the intermediate region 337 between neighboring traces 331. The dielectric material 360 can also include an upper portion (not shown in Figures 6 and 7) positioned between the upper surface 334 of the traces 331 and the remainder of the package support member 370a.

In a further aspect of an embodiment shown in Figures 6 and 7, the lower portion 362 of the dielectric material 360 does not cover the inner bond pads 353a or the outer bond pads 353b allow for electrical coupling to these bond pads. Alternatively, the dielectric material 360 can initially cover the bond pads 353a, 353b and can then be locally removed from the bond pads for electrical coupling. In either embodiment, the dielectric material 360 can reduce the capacitive coupling between adjacent traces 331 by reducing the dielectric constant of the intermediate region 337 between neighboring traces 331. For example, in some conventional arrangements, a solder mask material having a dielectric

constant of 3.5 or greater is positioned between neighboring traces 331. In one aspect of an embodiment shown in Figures 6 and 7, the dielectric material 360 can have a dielectric constant of less than 3.5, and in a specific embodiment, the dielectric material can be from about 1.0 to about 2.0.

In another aspect of an embodiment shown in Figures 6 and 7, the dielectric material 360 can fill less than the entirety of each intermediate region 337, leaving gaps that can be filled with air, helium, argon or another low-dielectric gas in a manner generally similar to that described above with reference to Figure 5B. In still further embodiments, the dielectric material 360 can be disposed on the traces 331 in accordance with any of the methods described above with reference to Figures 2-5D. Accordingly, an advantage of any of the embodiments of the packaged device 320 shown in Figures 6 and 7 is that the likelihood for capacitive coupling between adjacent traces 331 can be reduced or eliminated.

From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except by the appended claims.

CLAIMS

1. A method for packaging a microelectronic substrate, comprising:

positioning a conductive member at least proximate to the microelectronic substrate, the conductive member having first and second neighboring conductive portions with at least part of the first conductive portion separated from the neighboring second conductive portion to define an intermediate region between the conductive portions;

electrically coupling the first conductive portion of the conductive member to a first coupling site of the microelectronic substrate and electrically coupling the second conductive portion of the conductive member to a second coupling site of the microelectronic substrate; and

providing a dielectric material in the intermediate region between the conductive portions, the dielectric material having a dielectric constant less than about 3.5.

2. The method of claim 1 wherein the conductive portions each have a first surface adjacent to the microelectronic substrate, a second surface facing opposite the first surface, and a third surface between the first and second surfaces, and wherein the method further comprises providing the dielectric material adjacent to the third surfaces of the conductive portions.

3. The method of claim 1 wherein the conductive portions each have a first surface adjacent to the microelectronic substrate, a second surface facing opposite the first surface, and a third surface between the first and second surfaces, and wherein the method further comprises disposing the dielectric material on the second surfaces of the conductive portions and applying a force normal to the second surface to displace at least some of the dielectric material into the intermediate region between the conductive portions adjacent to the third surfaces of the conductive portions.

4. The method of claim 1 wherein positioning the conductive member includes positioning a leadframe adjacent to the microelectronic substrate, and wherein the

method further comprises providing the dielectric material between neighboring leadfingers of the leadframe.

5. The method of claim 1 wherein positioning the conductive member includes positioning adjacent to the microelectronic substrate a printed circuit board having conductive traces, and wherein the method further comprises providing the dielectric material between the conductive traces of the printed circuit board.

6. The method of claim 1, further comprising adhering a layer of the dielectric material to the conductive member.

7. The method of claim 1, further comprising:

disposing the dielectric material on the conductive member; and

applying heat and/or pressure to the dielectric material after disposing the dielectric material on the conductive member.

8. The method of claim 1, further comprising disposing the dielectric material on the conductive member in a liquid or vapor phase.

9. The method of claim 1 wherein electrically coupling the conductive portions of the conductive member to coupling sites of the microelectronic substrate includes attaching wire bonds between the conductive portions of the conductive member and bond pads of the microelectronic substrate.

10. The method of claim 1, further comprising disposing an encapsulating material over at least part of the conductive member and the microelectronic substrate.

11. The method of claim 1, further comprising selecting the dielectric constant of the dielectric material to be from about 1.0 to about 2.0.

12. The method of claim 1, further comprising selecting the dielectric material to include Teflon™.

13. A method for processing a circuit board for coupling to a microelectronic substrate, comprising:

providing a circuit board having a first conductive trace with a portion spaced apart from a corresponding portion of a second conductive trace to define an intermediate region between the first and second conductive traces; and

disposing in the intermediate region between the conductive traces a dielectric material having a dielectric constant less than approximately 3.5.

14. The method of claim 13, further comprising selecting the dielectric material to have a dielectric constant of from about 1.0 to about 2.0.

15. The method of claim 13, further comprising selecting the dielectric material to include a gas.

16. The method of claim 13, further comprising selecting the dielectric material to include gas, argon and/or helium.

17. The method of claim 13 wherein the conductive traces each have a first surface, a second surface facing opposite the first surface, and a third surface between the first and second surfaces with the third surface of the first conductive trace facing the third surface of the second conductive trace, and wherein the method further comprises disposing the dielectric material on the second surfaces of the conductive traces and applying a force normal to the second surfaces to displace at least some of the dielectric material into the intermediate region between the conductive traces adjacent to the third surfaces of the conductive traces.

18. The method of claim 13 wherein disposing the dielectric material includes adhering a layer of the dielectric material to the conductive member.

19. The method of claim 13, further comprising applying heat and/or pressure to the dielectric material after disposing the dielectric material on the conductive traces.

20. The method of claim 14 wherein disposing the dielectric material includes disposing the dielectric material in liquid or vapor phase.

21. A method for processing a leadframe for coupling to microelectronic substrates, comprising:

providing a leadframe having first and second connected leadfingers, at least a portion of the first leadfinger being separated from a neighboring portion of the second leadfinger, each leadfinger having a first surface, a second surface opposite the first surface, and a third surface between the first and second surfaces, the second surface having a bond site for receiving wire bonds; and

applying to the leadframe a dielectric material having a dielectric constant of less than about 3.5, the dielectric material being positioned adjacent to the third surfaces of the leadfingers and/or proximate to the third surfaces to extend between the third surfaces of the first and second leadfingers when the leadframe is connected to a microelectronic substrate.

22. The method of claim 21 wherein disposing the dielectric material includes disposing a pliable dielectric material on at least one of the first and second surfaces adjacent to the third surface.

23. The method of claim 21 wherein disposing the dielectric material includes disposing a first dielectric material on one of the surfaces of the leadfingers, further comprising disposing a second dielectric material different than the first dielectric material on another surface of the leadfingers.

24. The method of claim 21 wherein disposing the dielectric material includes disposing a pliable dielectric material on at least one of the first and second surfaces

adjacent to the third surface, and wherein the method further comprises applying a normal force to the at least one of the first and second surfaces to displace a portion of the dielectric material to a point between the third surfaces of the first and second leadfingers.

25. The method of claim 21, further comprising:

attaching a wire bond to the first leadfinger before disposing the dielectric material; and

disposing the dielectric material on the wire bond.

26. The method of claim 21, further comprising completely filling in a region between the third surface of the first leadfinger and the third surface of the neighboring second leadfinger.

27. The method of claim 21 wherein disposing the dielectric material includes dipping the leadframe into a volume of the dielectric material.

28. The method of claim 21 wherein disposing the dielectric material includes disposing the dielectric material in liquid or vapor phase.

29. A method for packaging a microelectronic substrate, comprising:

positioning leadfingers of a leadframe adjacent to corresponding bond sites of the microelectronic substrate;

electrically coupling the leadfingers to the bond sites;

disposing a first dielectric material adjacent to first surfaces of the leadfingers and the microelectronic substrate;

disposing a second dielectric material adjacent to second surfaces of the leadfingers facing opposite the first surfaces; and

introducing at least some of the first and/or second dielectric material into a gap between adjacent leadfingers by biasing the leadframe toward the microelectronic substrate and/or applying heat to at least one of the dielectric materials.

30. The method of claim 29 wherein biasing the leadframe includes applying a normal force to the at least one of the first and second surfaces of the leadfingers.

31. The method of claim 29 wherein disposing the first dielectric material includes adhering a layer of the first dielectric material adjacent to the first surfaces of the leadfingers.

32. The method of claim 29 wherein disposing the first dielectric material includes applying a layer of adhesive to the first dielectric material and adhering the adhesive layer to the microelectronic substrate.

33. The method of claim 29 wherein disposing the first dielectric material includes depositing particles of the first dielectric material to form a layer of the first dielectric material.

34. The method of claim 29, further comprising:

removing a portion of the second dielectric material from the second surface of each leadfinger to expose a portion of the second surface of each leadfinger; and

attaching wire bonds between the exposed portions of the leadfingers and the bond pads.

35. The method of claim 29, further comprising:

leaving portions of the second surfaces of the leadfingers uncovered by the second dielectric material; and

attaching wire bonds between the bond sites of the microelectronic substrate and the uncovered portions of the leadfingers.

36. The method of claim 29 further comprising selecting the first and second dielectric materials to have approximately the same dielectric constant.

37. The method of claim 29, further comprising:

disposing an encapsulating material adjacent to the leadframe and the microelectronic substrate; and

selecting at least one of the first and second dielectric materials to have a dielectric constant less than a dielectric constant of the encapsulating material.

38. The method of claim 29, further comprising selecting at least one of the first and second the dielectric materials to have a dielectric constant less than about 3.5.

39. The method of claim 29, further comprising selecting the first dielectric material to have a dielectric constant of from about 1.0 and to about 2.0.

40. A conductive structure for coupling to a microelectronic substrate, comprising:

a conductive member having first and second conductive portions, at least a part of the first conductive portion being spaced apart from a neighboring part of the second conductive portion to define an intermediate region between the first and second conductive portions, each conductive portion having a bond region positioned to electrically couple to a microelectronic substrate when the conductive member is positioned at least proximate to the microelectronic substrate; and

a dielectric material adjacent to the first and second conductive portions, the dielectric material having a dielectric constant less than about 3.5.

41. The conductive structure of claim 40 wherein the conductive member includes a leadframe, the first conductive portion includes a first leadfinger of the leadframe and the second conductive member includes second leadfinger connected to the first leadfinger.

42. The conductive structure of claim 40 wherein the conductive member includes an assembly of conductive traces, the first conductive portion includes a first conductive trace and the second conductive portion includes a second conductive trace with

at least a portion of the first trace spaced apart from a portion of the second trace, and wherein the conductive structure further comprises a printed circuit board supporting the first conductive trace relative to the second conductive trace.

43. The conductive structure of claim 40 wherein the conductive portions each have a first surface, a second surface facing opposite the first surface, and a third surface between the first and second surfaces, and wherein the dielectric material is adjacent to the third surfaces of the conductive portions.

44. The conductive structure of claim 40 wherein the conductive portions each have a first surface, a second surface facing opposite the first surface, and a third surface between the first and second surfaces, and wherein the dielectric material includes a pliable dielectric material disposed at a position on the second surfaces of the conductive portions proximate to the third surfaces.

45. The conductive structure of claim 40 wherein the dielectric material includes a thermoset material.

46. The conductive structure of claim 40 wherein the conductive portions each have a first surface, a second surface facing opposite the first surface, and a third surface between the first and second surfaces, and wherein the dielectric material is a first dielectric material adjacent one of surfaces of the conductive portions, and wherein the conductive structure further includes a second dielectric material different than the first dielectric material adjacent to another of the surfaces.

47. The conductive structure of claim 40 wherein the dielectric material is adhesively attached to the conductive member.

48. The conductive structure of claim 40 wherein the dielectric material includes a gas.

49. The conductive structure of claim 40 wherein the dielectric material includes air, argon and/or helium.

50. A microelectronic device package, comprising:

a microelectronic substrate;

a conductive member at least proximate to the microelectronic substrate, the conductive member having first and second conductive portions, at least a part of the first conductive portion being spaced apart from a neighboring part of the second conductive portion, each conductive portion having a bond region proximate to the microelectronic substrate;

a first conductive connector connected between the microelectronic substrate and the bond region of the first conductive portion;

a second conductive connector connected between the microelectronic substrate and the bond region of the second conductive portion; and

a dielectric material between the first and second conductive portions, the dielectric material having a dielectric constant less than about 3.5.

51. The package of claim 50, further comprising an encapsulating material adjacent to the microelectronic substrate and the conductive member.

52. The package of claim 50 wherein the dielectric material is a first dielectric material, and wherein the package further comprises a second dielectric material at least partially encapsulating the microelectronic substrate, the conductive member, and the conductive connectors and having a chemical composition generally the same as a chemical composition of the first dielectric material.

53. The package of claim 50, further comprising an encapsulating material adjacent to the microelectronic substrate and having a dielectric constant greater than the dielectric constant of the dielectric material.

54. The package of claim 50 wherein the dielectric material includes a gas.

55. The package of claim 50 wherein the first conductive connector includes a first wire bond and the second conductive connector includes a second wire bond.

56. The package of claim 50 wherein the first and second conductive portions define an intermediate region therebetween and the dielectric material fills the entire intermediate region.

57. A microelectronic device package, comprising:

a microelectronic substrate having a first face, a second face facing opposite the first face, and a plurality of terminals at the first face;

a leadframe positioned adjacent to the first surface, the leadframe having a plurality of leadfingers, each leadfinger having a first portion coupled to the leadframe and a second portion spaced apart from an adjacent leadfinger; each leadfinger having a first surface facing toward the first face of the microelectronic substrate, a second surface facing opposite the first surface, and a third surface between the first and second surfaces;

a dielectric material having a first dielectric constant and being disposed adjacent to the leadframe, the dielectric material being engaged with the first, second and third surfaces of the leadfingers; and

an encapsulating material at least partially surrounding the leadfingers and the microelectronic substrate, the encapsulating material having a second dielectric constant higher than the first dielectric constant.

58. The package of claim 57, further comprising an adhesive between the leadfinger and the dielectric material to secure the dielectric material to the leadfinger.

59. The package of claim 57 wherein the first dielectric constant of the dielectric material is less than about 3.5.

60. The package of claim 57 wherein the first dielectric constant of the dielectric material is from about 1.0 to about 2.0.

METHOD AND APPARATUS FOR DECOUPLING CONDUCTIVE PORTIONS OF A MICROELECTRONIC DEVICE PACKAGE

ABSTRACT

A method and apparatus for decoupling conductive portions of a microelectronic device package. In one embodiment, the package can include a microelectronic substrate and a conductive member positioned at least proximate to the microelectronic substrate. The conductive member can have first and second neighboring conductive portions with at least a part of the first conductive portions spaced apart from a part of the neighboring second conductive portion to define an intermediate region between the first and second conductive portions. Each conductive portion has a bond region electrically coupled to the microelectronic substrate. A dielectric material is positioned adjacent to the first and second conductive portions in the intermediate region and has a dielectric constant of less than about 3.5.

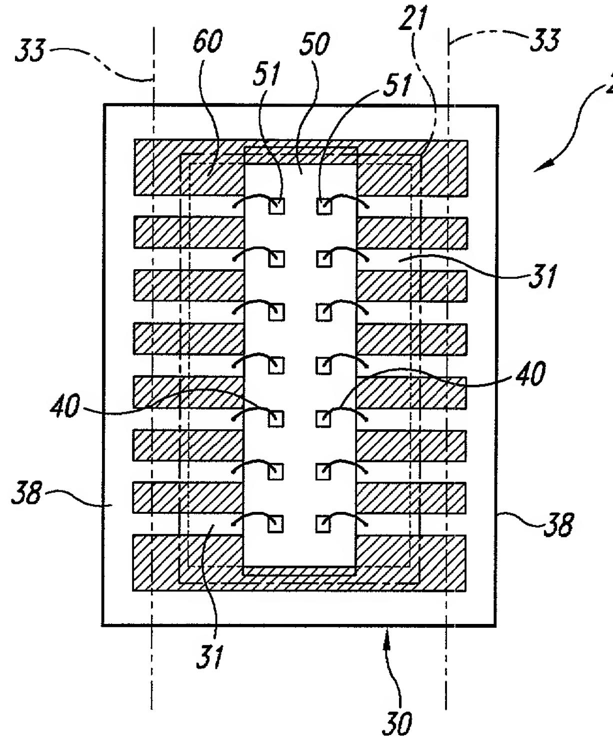

Fig. 1
(Prior Art)

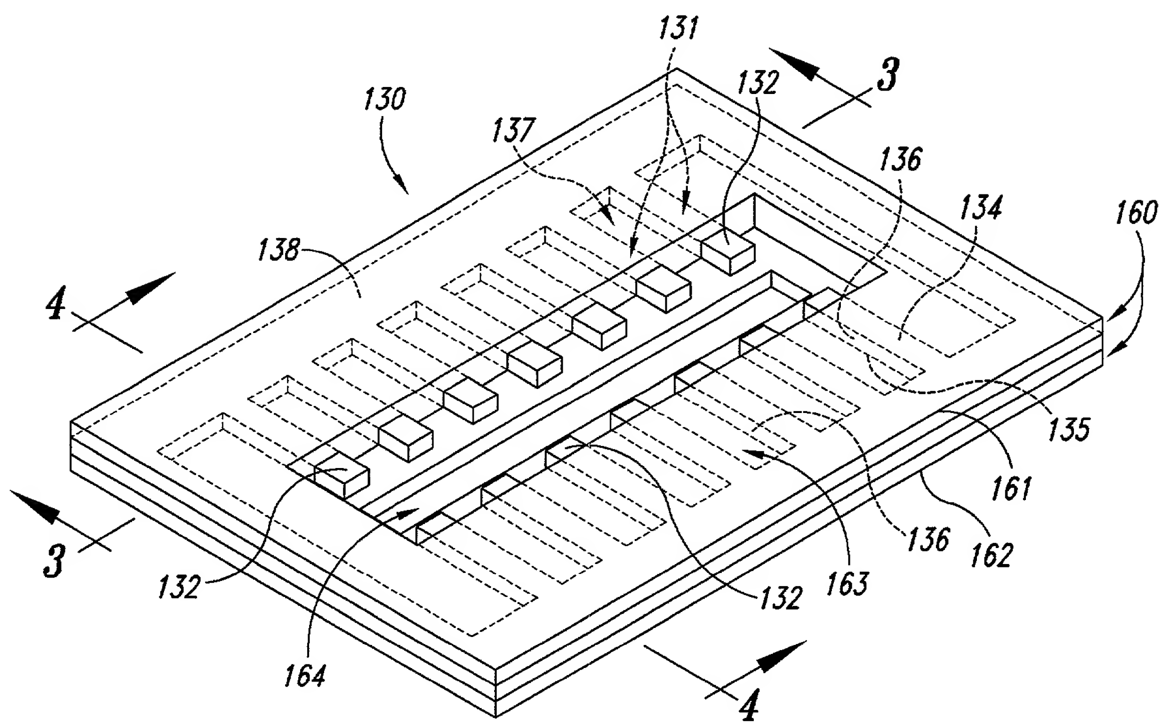

Fig. 2

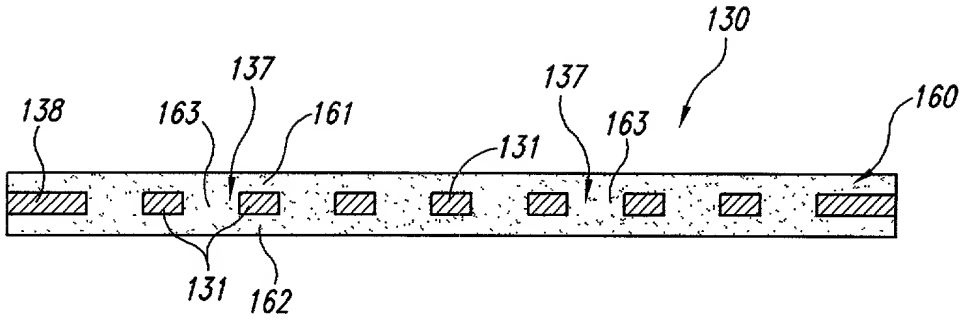
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Fig. 3

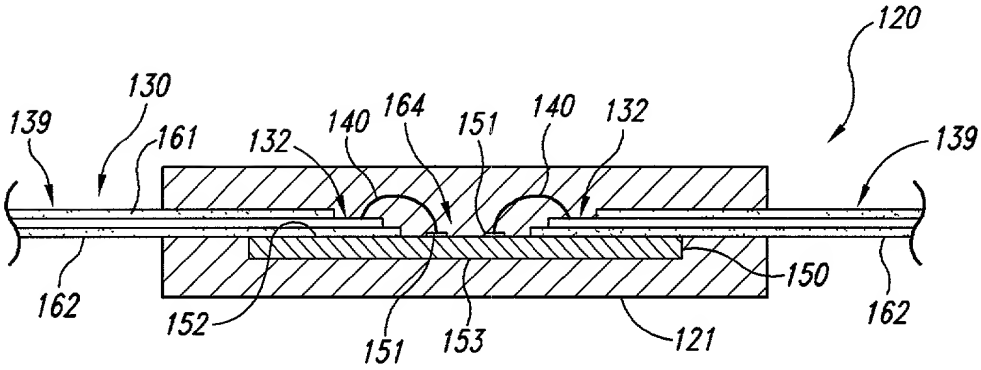
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Fig. 4

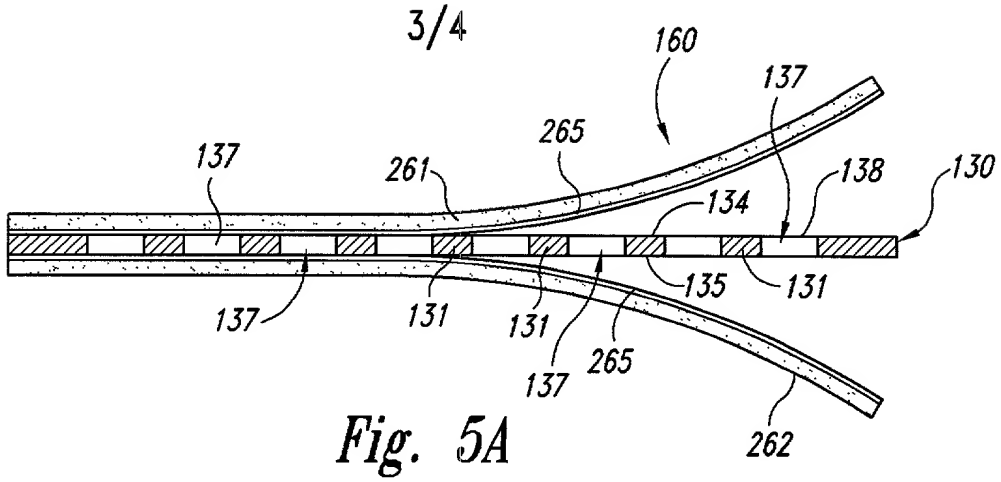

Fig. 5A

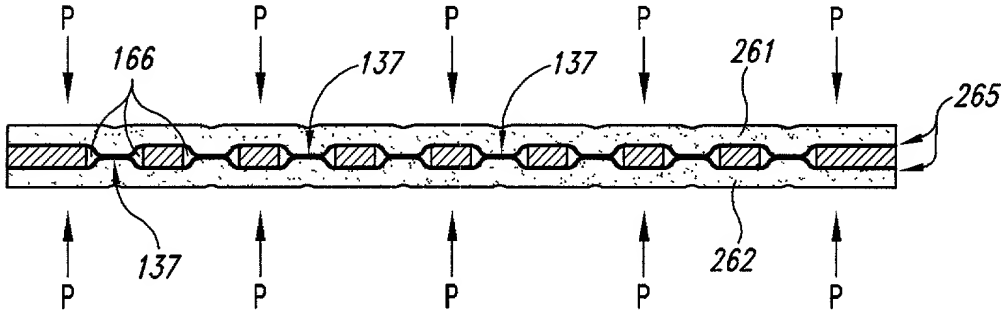

Fig. 5B

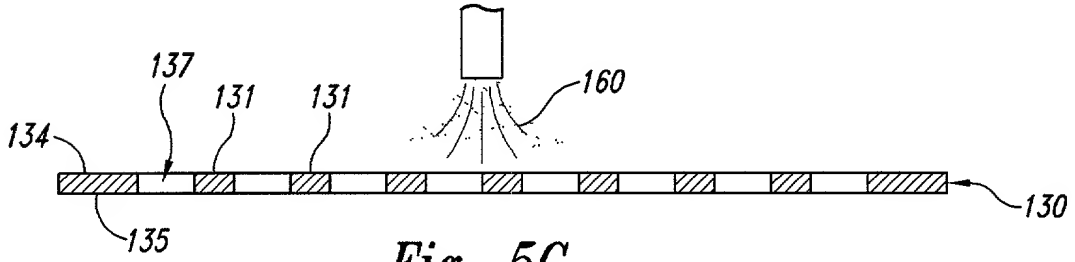

Fig. 5C

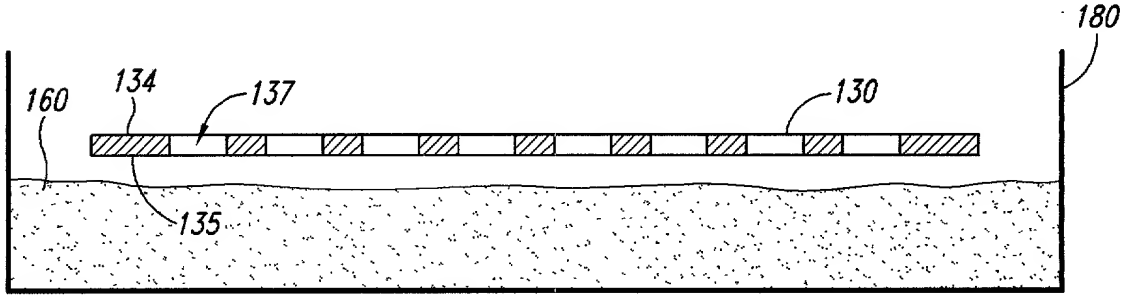

Fig. 5D

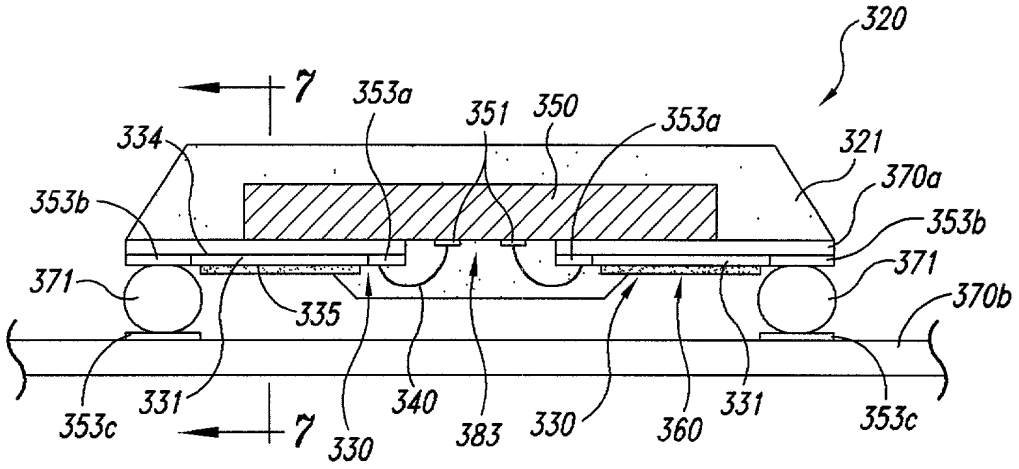
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Fig. 6

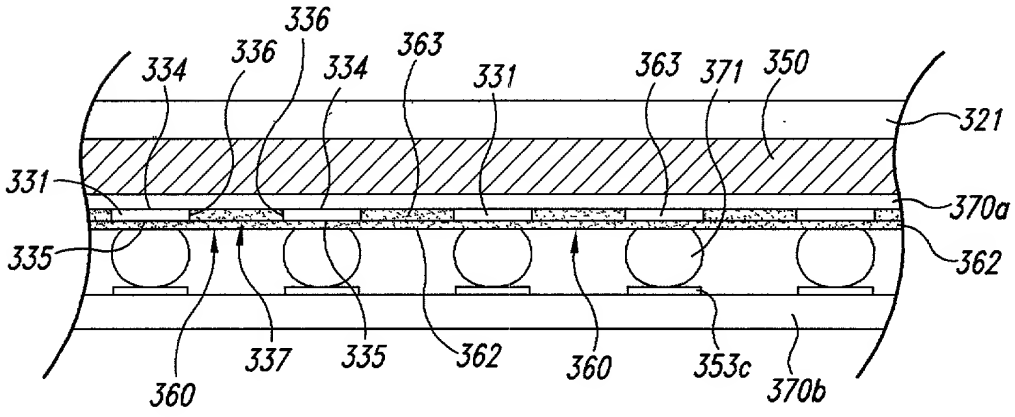
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Fig. 7

DECLARATION

As the below-named inventors, we declare that:

Our residences, post office addresses, and citizenships are as stated below under our names.

We believe we are the original, first, and joint inventors of the subject matter claimed and for which a patent is sought on the invention entitled "METHOD AND APPARATUS FOR DECOUPLING CONDUCTIVE PORTIONS OF A MICROELECTRONIC DEVICE PACKAGE" in the foregoing specification and claims.

We have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to above.

We acknowledge our duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. § 1.56(a).

We further declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that the making of willfully false statements and the like is punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from this patent application.

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	David J. Corisis and Aaron M. Schoenfeld
Filed	:	Concurrently herewith
For	:	METHOD AND APPARATUS FOR DECOUPLING CONDUCTIVE PORTIONS OF A MICROELECTRONIC DEVICE PACKAGE
		Docket No. : 108298531US

Box Patent Application
Assistant Commissioner for Patents
Washington, DC 20231

ELECTION UNDER 37 C.F.R. §§ 3.71 AND 3.73 AND POWER OF ATTORNEY

Sir:

The undersigned, being Assignee of the entire interest in the above-identified application by virtue of an Assignment filed concurrently herewith, hereby elects, under 37 C.F.R. § 3.71, to prosecute the application to the exclusion of the inventor.

Assignee hereby appoints JERRY A. RIEDINGER, Registration No. 30,582; MAURICE J. PIRIO, Registration No. 33,273; JOHN C. STEWART, Registration No. 40,188; MICHAEL D. BROADDUS, Registration No. 41,637; BRIAN P. MCQUILLEN, Registration No. 41,989; TARANEH MAGHAME, Registration No. 43,768; CATHERINE HONG TRAN, Registration No. 43,960; ROBERT G. WOOLSTON, Registration No. 37,263; PAUL T. PARKER, Registration No. 38,264; JOHN M. WECHKIN, Registration No. 42,216; CHRISTOPHER DALEY-WATSON, Registration No. 34,807; STEVEN D. LAWRENZ, Registration No. 37,376; JAMES A.D. WHITE, Registration No.

43,985; FRANK ABRAMONTE, Registration No. 38,066, along with MICHAEL L. LYNCH, Reg. No. 30,871; WALTER D. FIELDS, Reg. No. 37,130; CHARLES B. BRANTLEY, II, Reg. No. 38,086; KEVIN D. MARTIN, Reg. No. 37,882; and DAVID J. PAUL, Reg. No. 34,692, of Micron Technology, Inc., 8000 South Federal Way, Boise, Idaho 83706-9632 as the principal attorneys with full power of substitution, association, and revocation to prosecute said application, to transact all business in the Patent and Trademark Office connected therewith, and to receive the letters patent therefor. Please direct all direct all telephone calls to John M. Wechkin at (206) 583-8888 and telecopies to (206) 583-8500.

Please direct all communications to:

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1201 Third Avenue, Suite 4800
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Attn: John M. Wechkin

Pursuant to 37 C.F.R. § 3.73, the undersigned duly authorized designee of Assignee certifies that the evidentiary documents have been reviewed, specifically the Assignment to MICRON TECHNOLOGY, INC., filed concurrently herewith for recording, a copy of which is attached hereto, and certifies that to the best of my knowledge and belief, title remains in the name of the Assignee.

MICRON TECHNOLOGY, INC.

8-18-00
DATE

Michael L. Lynch
Chief Patent Counsel

Enclosure:
Copy of Assignment